# Homework Four Solutions

1.

7)a) Could use only $V_{DD}$ or gnd on MOSFET sources. Better to use MUX-based design style. Need buffer or inverter on output to restore. Inverters more efficient in CMOS, so start from $\bar{f}$.

$$f(a,b,c) = ab + \bar{a}\bar{b}\bar{c}$$

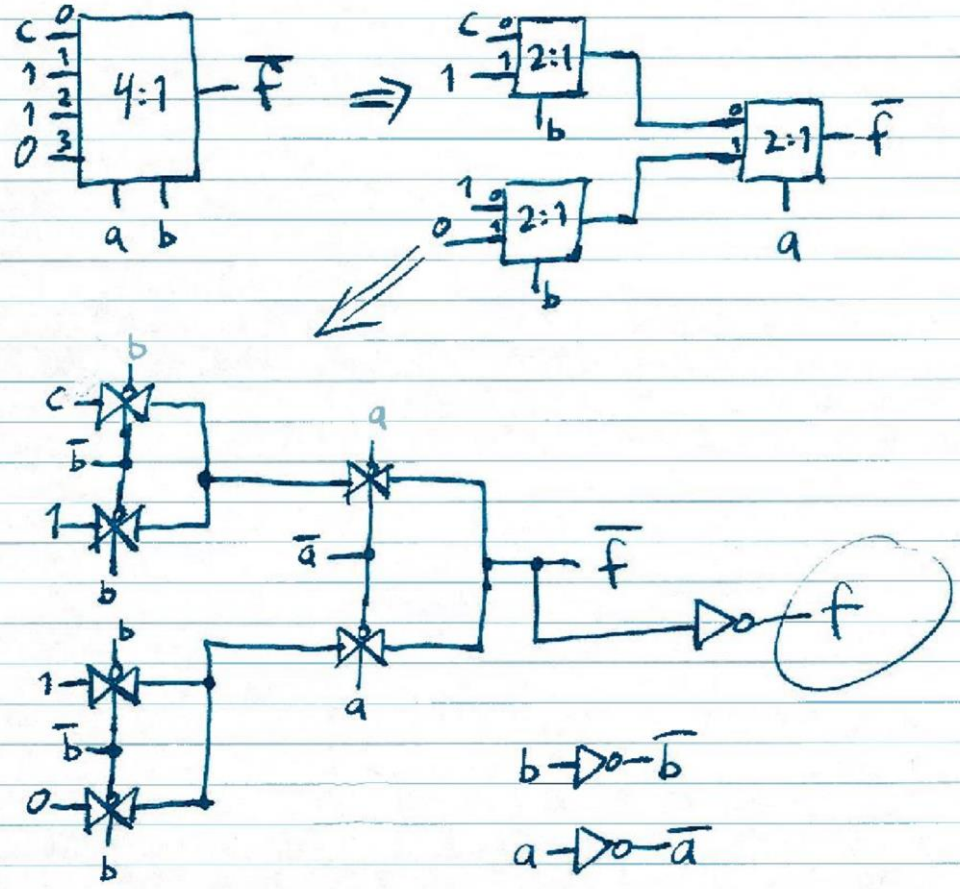
$$\bar{f}(a,b,c) = \overline{ab + \bar{a}\bar{b}\bar{c}}$$

$$= \overline{ab} \cdot \overline{\bar{a}\bar{b}\bar{c}}$$

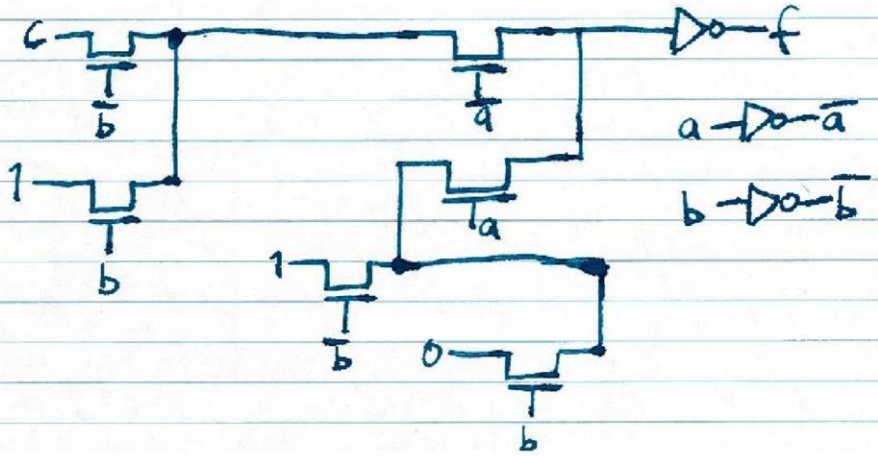
$$= (\bar{a}+\bar{b})(a+b+c)$$

| a | b | c | $(\bar{a}+\bar{b})(a+b+c)$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 |

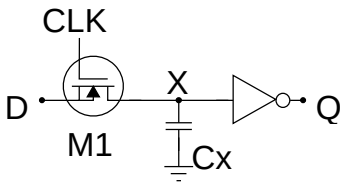
7)a) cont.)




7)b) Starting from soln. to 7)a).



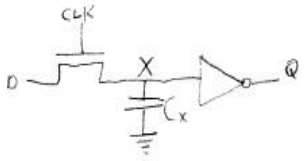
2. In the latch in the following figure, compute the setup time when $D$ is low (that is, a low value is being passed from $D$ to $X$). Assume the initial voltage at node $X$ is $(V_{DD} - V_{Tn}(V_x)) = 1.8$ V. You must compute the equivalent resistance of the pass transistor at the midpoint of the voltage swing of interest. Let the width of the NMOS pass transistor be W=1μm and the PMOS/NMOS sizes of the inverter are 2μm and 1μm respectively. Use the 0.6fF/μm junction capacitance assumption and ignore overlap capacitance.




The NMOS pass transistor is in velocity saturation at the voltage of interest (0.9 V). However, this was not noted during office hours, so we will accept solutions which assume the linear region.

Multiple methods of computing Idsat are given in the text. Any of these methods is acceptable. The following solution shows just one.

1)




We assume that a 'low' value is stored at X when $V_x$ has fallen to 0.9V (assume $V_m$ for the inverter is 1.25V)

we must find the time required for $V_x$ to fall from 1.8V to 0.9V.

Total cap at X is composed of three parts, junction cap from the pass transistor and the 2 gate caps from the inverter.

$C_{junc} = 0.6\,fF/\mu m \cdot 1\mu m = 0.6\,fF$

The Nmos in the inverter is in the linear region initially
The pmos is in saturation.

$C_{gnmos} = C_{ox} WL = 6\,fF/\mu m^2 \cdot 1\mu m \cdot 0.25\mu m = 1.5\,fF$

$C_{gpmos} = \frac{2}{3} C_{ox} WL = \frac{2}{3} \cdot 6\,fF/\mu m^2 \cdot 2\mu m \cdot 0.25\mu m = 2\,fF$

$C_x = 0.6 + 1.5 + 2 = 4.1\,fF$

We are told to compute $R_{eq}$ of the pass trans. at 0.9V

$R_{eq} = \frac{V}{I}$

$V = 0.9V$ $\quad V_{ds} = 0.9 > 0.63$ so the transistor is in velocity saturation

$I_{ds} = k_n' \frac{W}{L}\left((V_{gs} - V_T)V_{DSAT} - \frac{V_{DSAT}^2}{2}\right)$ page 97, eq. 3.38

$I_{DS} = 5.1 \cdot 10^{-4}\,A$

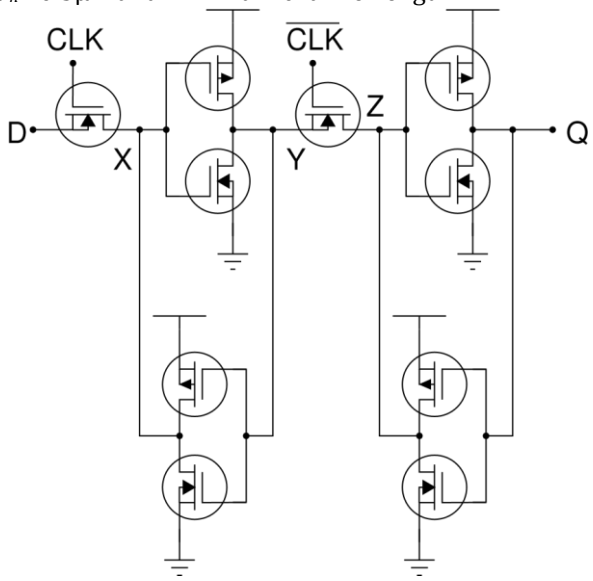
$R_{eq} = 1.770\,k\Omega$

$t_p$ for $\left(V_x = \frac{1.8}{2}\right)$ is $0.69RC$

$t_p = 5\,ps$

setup time is 5ps

3. Assume the register shown below is driven at input $D$ by a CMOS inverter. A 4 cross-coupled inverters in the flip-flop have $W_p$=$W_n$= 0.5µm and minimum channel length.

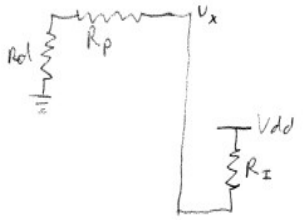



(a) Find a sizing constraint (or relationship between) on the inverter driving node $D$ ( not shown explicitly in the diagram) and the NMOS pass transistor that ensures proper functionality for storing a 0 (ignore body effect) at $Q$. You may need to make some simplifying assumptions regarding feedback please describe these clearly in your answer. Take the switching voltage, $V_M$ = 1V for the inverters with $W_p$ = $W_n$ and the default technology parameters.

2) Assume $V_x$ is initially $V_{dd}$.

a) In order for the first latch to switch and store a 0, $V_x$ must fall below $V_m$ of the upper inverter.

Drawing the three transistors driving net X (as resistors) we have




Note than $R_p$ is unshown on the transistor schematic.

$$V_x = V_{dd} \cdot \left(\frac{R_d + R_p}{R_d + R_p + R_I}\right)$$

$V_x < V_m$

$V_x \leq 1V$

$V_{dd} = 2.5V$

$$1 > 2.5\left(\frac{R_d + R_p}{R_d + R_p + R_I}\right)$$

$$\boxed{(R_d + R_p) \leq \frac{2}{3} R_I}$$

$R \propto \frac{1}{width}$ so this is essentially a constraint of sizing

$R_I$ is $\sim \frac{31}{2} k\Omega$ as given in the book, or you calculate $R_{eq}$ using $V = IR$ at the $V_x = 1V$ point.

$(R_d + R_p) < 10.\bar{3}\, k\Omega$

(b) How would you redesign the flip-flop to relax the sizing requirement on the driving stage? (qualitative answer is sufficient)

If the lower inverter is sized-down, $R_I$ will be larger and thus the driver and pass transistor can be made weaker (smaller) while still satisfying the requirement from 2 a.

(c) Suppose we change the circuit by adding a feedback NMOS pass transistor controlled by inserted between the output of the feedback inverter in the leading stage and node *X* (the leading stage now looks like Figure 7-8a of the text). How does this change the sizing requirement of part (a)? A qualitative answer is sufficient.

Breaking the feedback loop prevents the fight at net X. This effectively removes the sizing constraint. The timing properties will be still be dependent on the size of the driver and pass transistor, but the functional behavior will not.

4. To perform a certain function in a microprocessor, data must propagate through 100 stages of logic, each having a delay equal to that of an inverter, $t_{inv}$. The speed of this operation sets the clock frequency of the system.

(a) Compare the speed (quantified by maximum clock frequency) of a non-pipelined system to that of a pipelined system with 10 stages. Let the design use registers having a delay equal to $3t_{inv}$ and a set-up time of $3t_{inv}$ also.

The following solution assumes that no registers are placed at the beginning or end of the system. We will also accept solutions which do place registers at the beginning and end (i.e., $t_{comb} = 106 \cdot t_{inv}$).

$f_{combmax} = 1/t_{comb} = 1/(100 \cdot t_{inv})$ $f_{pipemax} = 1/t_{pipe} = 1/(16 \cdot t_{inv})$

(b) What do the results imply about breaking up operations into an increasing number of very small operations?

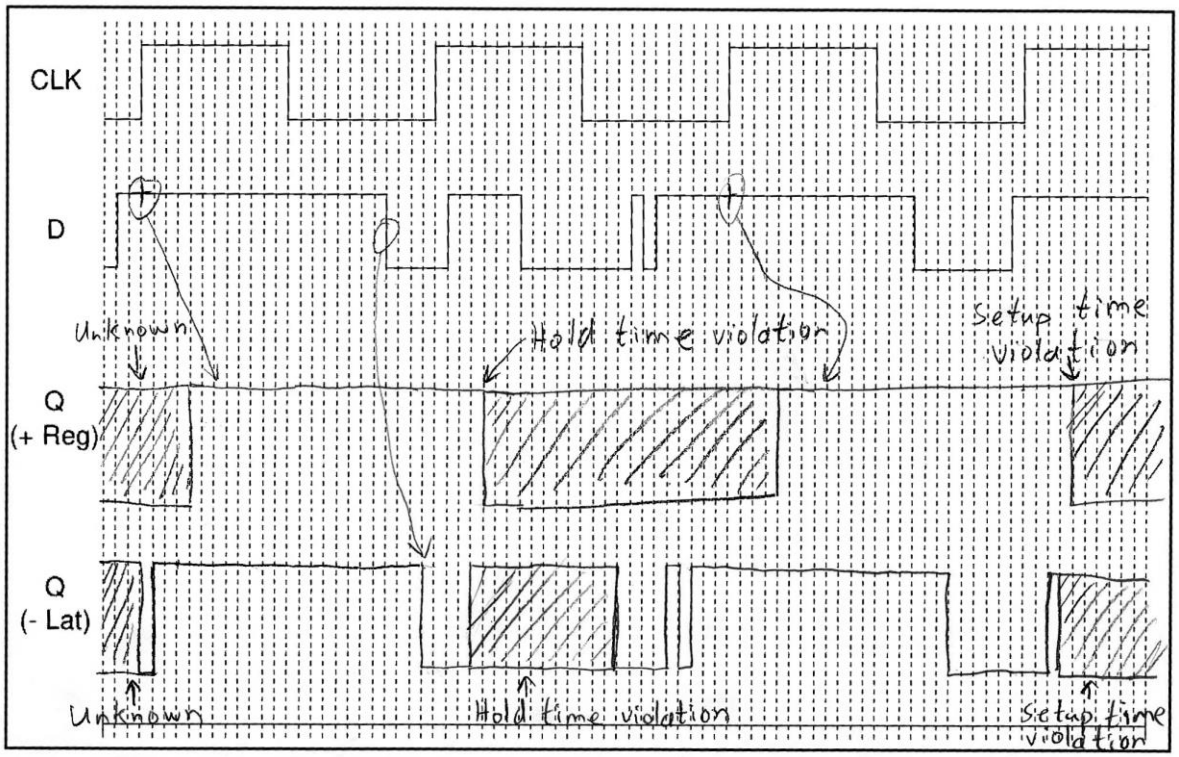
i. Pipelining increases throughput (clock frequency)
ii. Pipelining increases latency (due to the addition of register delays)
iii. If stages are too small, register delay dominates the combinational delay and there will be little improvement in throughput.

5. Given the following clock and data waveforms, draw the output waveforms for a

(a) positive edge-triggered register and

(b) a negative (or transparent-low) latch.

The timing characteristics of these sequential elements follow: $t_{c \to Q} = 4$ units, $t_{D \to Q} = 3$ units, $t_{setup} = t_{hold} = 2$ units. Vertical dashed lines have a separation of one unit. The clock period is equal to 24 units. Clearly mark on the figure where setup and hold time violations occur for each sequential element.



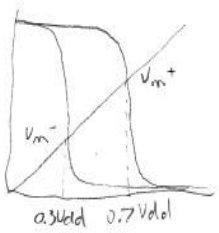
6. Consider a CMOS inverter driving a latch through a noisy wire. We expect noise voltage of up to 70% of $V_{DD}$ on either supply rail to be induced in the line. We need the input to this Latch to be "clean" or noise-free.

(a) Explain (in terms of a VTC) why a static CMOS inverter (or pair of inverters to make it non-inverting) will not be able to provide the required noise immunity if inserted before the Latch at the end of the wire.

The "high" output portion of the VTC needs to cover input voltages ranging from 0 – 0.7$V_{dd}$, while the "low" portion of the VTC needs to cover input voltages ranging from 0.3$V_{dd}$–$V_{dd}$. These ranges overlap, and thus are impossible in a simple inverter.

(b) Suppose we place a CMOS Schmitt trigger at the end of the line, before the latch. Size the controlling inverter (M3 and M4 in Figure 7-47 of the text) to ensure proper noise rejection assuming that both the input inverter and feedback inverter have $W_p$ = 2μm, $W_n$ = 1μm with minimum channel lengths.

7b)




$V_m = \frac{r V_{dd}}{1+r}$ with $r = \frac{k_p V_{DSAT_p}}{k_n V_{DSAT_n}}$ $\quad V_{m+} = 0.7 \cdot V_{dd} = \frac{r \cdot V_{dd}}{1+r}$ $\quad r_+ = 2.\overline{3}$

$V_{m-} = 0.3 \cdot V_{dd} = \frac{r \cdot V_{dd}}{1+r}$ $\quad r_- = 0.429$

When $V_{out}$ is low and m4 is on

$r_+ = \frac{k_p' \cdot \frac{1}{L} \cdot (2\mu m + X) \cdot -1}{k_n' \cdot \frac{1}{L} \cdot 1\mu m \cdot 0.63}$

$X = 3.635 \mu m$

m4 has width $3.635 \mu m$

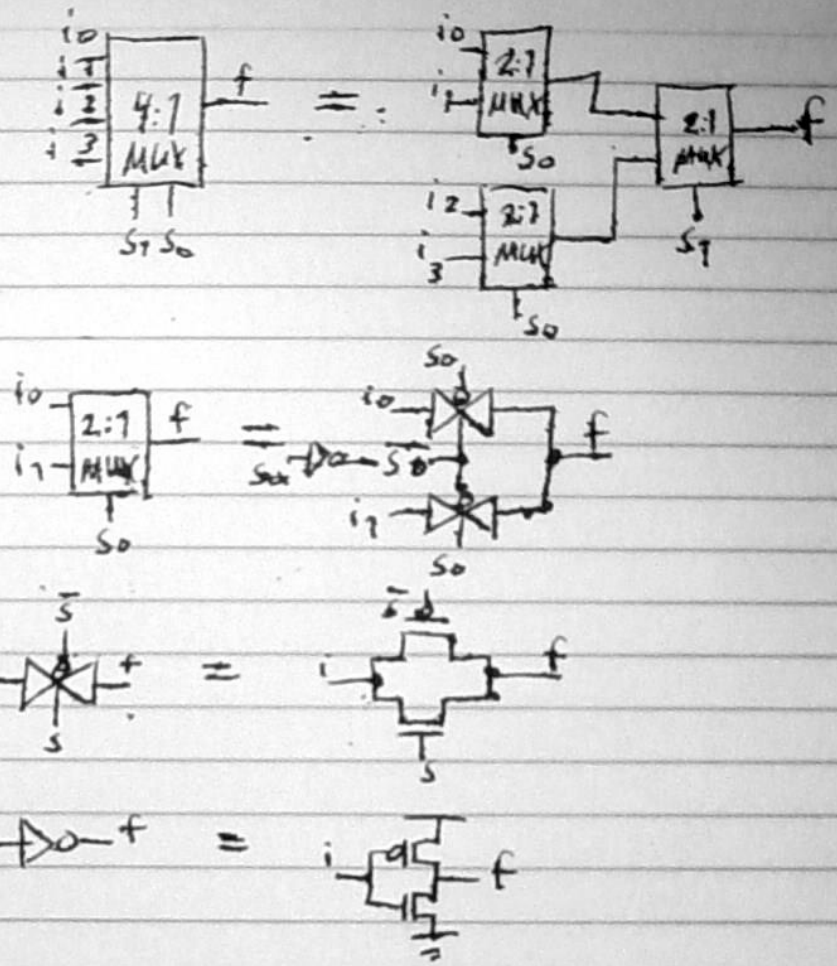
$r_- = \frac{k_p' \cdot \frac{1}{L} \cdot (2\mu m) \cdot -1}{k_n' \cdot \frac{1}{L} \cdot (1\mu m + x) \cdot 0.63}$

$x = 0.93$

m3 has width $0.93 \mu m$

7. Demonstrate that you know how to design a 4:1 MUX from the transistor level. Your design should have a structure making it possible to be sure that the maximum resistance from an output to $V_{DD}$ or $V_{SS}$ is no greater than that of a balanced, minimum-width inverter. You may size relative to *w*, the minimal width of a FET.

6)




All inputs will pass through two TGs before reaching the output, and we don't know the resistance to $V_{DD}$ or ground for the prior stage of logic. Therefore, we can most easily solve the problem by using an inverter on each input, and the output, or just double-inverting the output with balanced min-width inverters

8. What is the state of an asynchronous finite state machine the function of? What is the output of an asynchronous finite state machine the function of?
    - The next state is a function of the current state and the inputs.
    - The output is a function of the current state and the inputs.

9. Design a one-input circuit that will produce a constant output when its input is 0 and will produce an output that oscillates between 0 and 1 when its input is 1. Design and size this device such that the period of oscillation is approximately 5ns. Use transistors to supply any required resistance and capacitance.

    If we take a two-input NAND with one input connected to *I* and the other connected to the NAND's own output followed by a delay element, we will get the desired behavior. It still remains to make sure the delay is approximately half of the period, or 2.5ns. The propagation delay for a minimal-width inverter in the default process is approximately 50 ps (you can calculate that or find it . Therefore, we need 50 minimum-width inverters in the chain feeding back to the NAND gate's second input. It would have also been fine to use a more precise estimate of NMOSFET capacitance (such as those on page 201) for propagation delay calculation.

    Note that the main purpose of this exercise is to get you thinking about feedback paths and delays. There exist other ways to generate periodic oscillating signals that have more precise timing.

10.